Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2017**

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| **Code :** | **14EC2067** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VERILOG HDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. |  | Using Verilog HDL Top down methodology design 4- bit counter, also explain top down methodology with block diagram. | CO1 | 20 |
| (OR) | | | | |
| 2. |  | Explain Verilog HDL data operators. | CO2 | 20 |
| 3. | a. | With example explain the Structural model used in Verilog HDL. | CO2 | 14 |
|  | b. | Design the following circuit using Verilog HDL.  C:\Users\Office\Downloads\combinational.jpg | CO2 | 6 |
| (OR) | | | | |
| 4. |  | Discuss Timing controls in Verilog HDL. | CO3 | 20 |
| 5. | a. | Show the syntax of initial block and always statement. Write one example for each. | CO2 | 14 |
|  | b. | From the following initial block with blocking procedural assignments evaluate simulation time of each statement.  initial  begin  x=1'b0;  y= #10 1'b1;  z= # 5 1'b0;  w= #20 {a,b,c};  s=#5 1’b1;  end | CO1 | 6 |
| (OR) | | | | |
| 6. | a. | A simple module called D implements the following logic equations  out = (a+ b) . c  The gate level implementation is shown in module D. The module contains two gate delays 5 and 4 time units. Write the verilog definition for module D with Delay. | CO3 | 15 |
|  | b. | Show the syntax of multiway branching statement. | CO1 | 5 |
| 7. |  | Discuss briefly about the continuous assignment and procedural assignment statements. | CO1 | 20 |
| (OR) | | | | |
| 8. |  | Design RS and D flip flop using Verilog HDL | CO2 | 20 |
| **Compulsory:** | | | | |
| 9. | a. | Design Multiplexer using Verilog CMOS switches. | CO3 | 14 |
|  | b. | Mention the switches used in Verilog HDL. Discuss their functions. | CO3 | 6 |